

# U1 - KAL00

## Compal Confidential

### Schematics Document

### AMD S1g2/ ATI RS780M / SB700

Wednesday, January 16, 2008

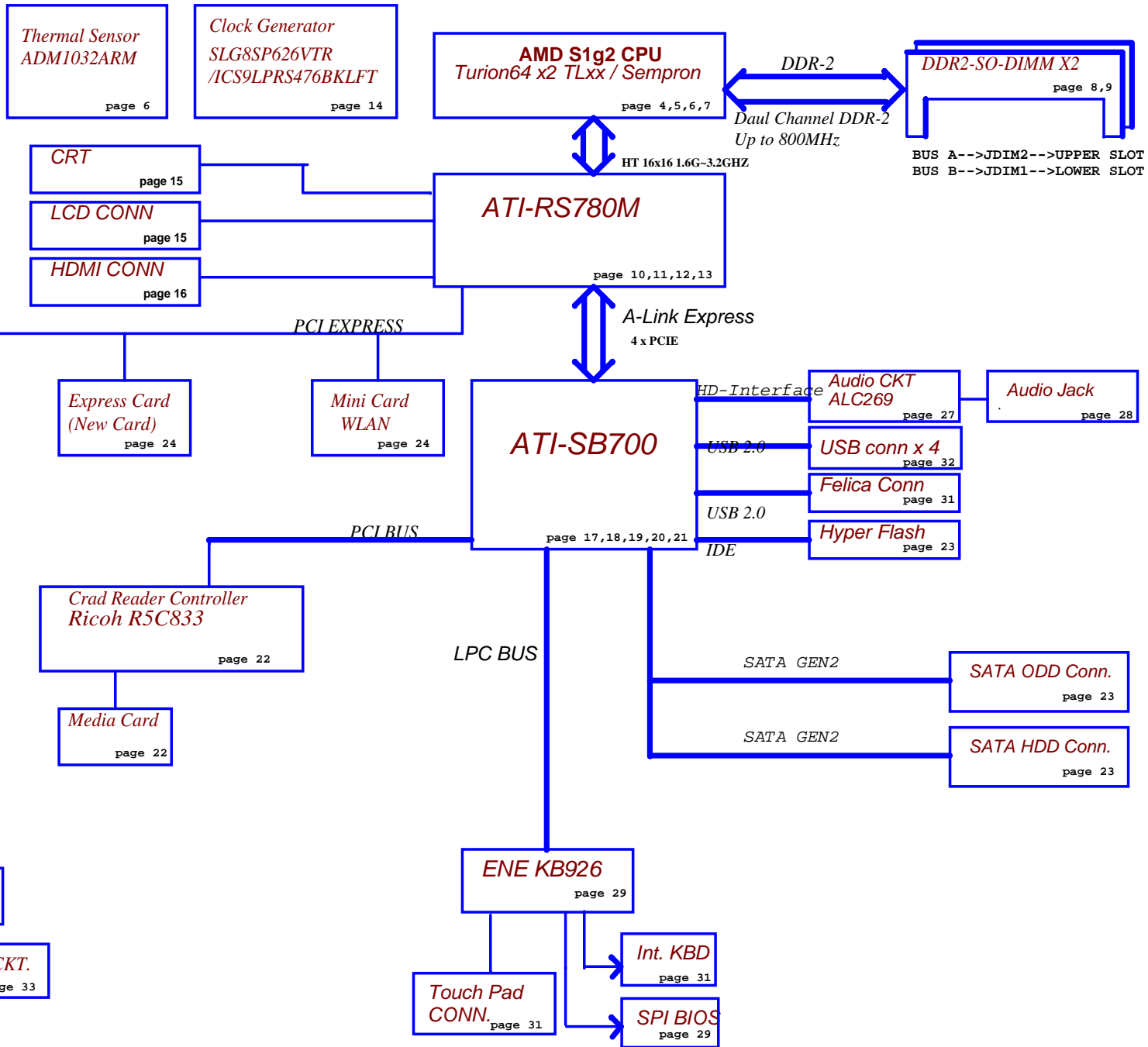
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Issued Date	2007/12/12	Deciphered Date	2008/12/12	Cover Sheet	
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Project Code: ANRKAL0000(KAL00)

File Name : LA-4381P

PCB P/N:



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Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE0,1	Core voltage for CPU	ON	OFF	OFF
+VDDNB	+0.8V~1.1V CPU NBVDD	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	1001 110X b?
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

Device	Address
Clock Generator (ICS9LPRS476BKLF)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM1	1001 010Xb?

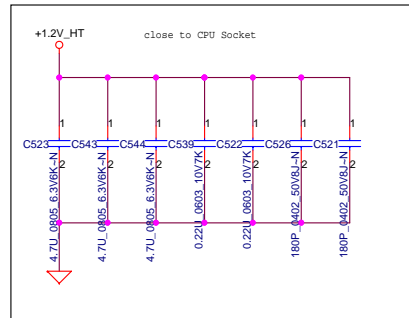
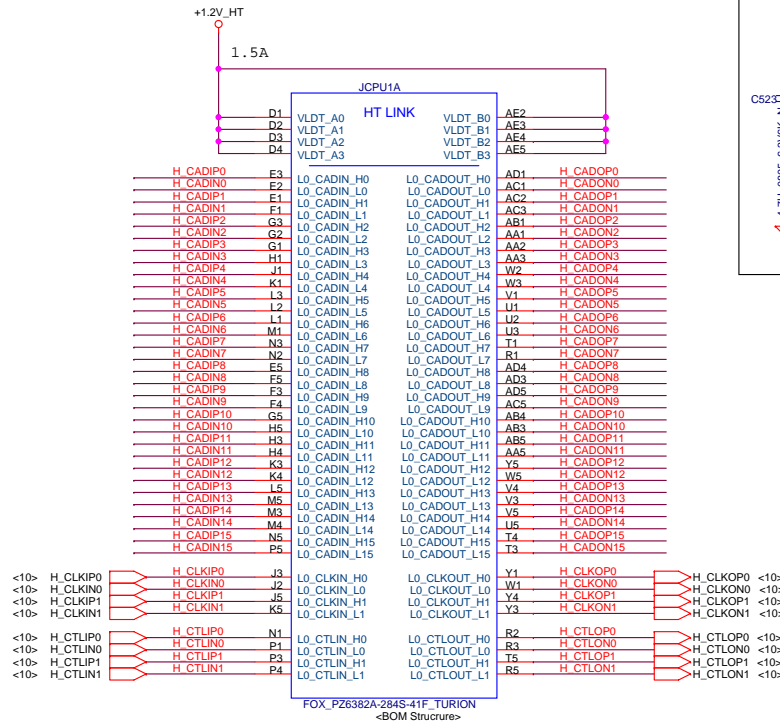
Board ID	PCB Revision
0	0.1 (U1 ES1)
1	0.2 (U1 ES2)
2	0.3 (U1 PP)
3	0.4 (U1 PPR)
4	1.0 (U1 IRT)
5	
6	
7	

[illegible]

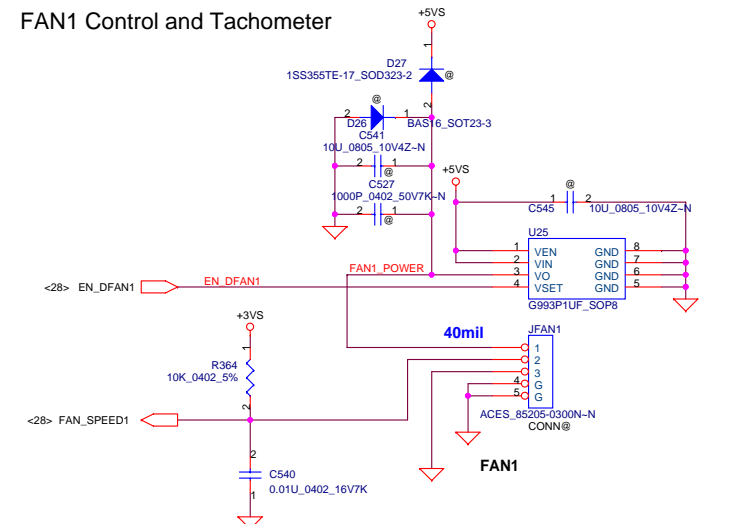
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<10> H\_CADIP[0..15] H\_CADIP[0..15]  
<10> H\_CADIN[0..15] H\_CADIN[0..15]

H\_CADOP[0..15] H\_CADOP[0..15] <10>  
H\_CADON[0..15] H\_CADON[0..15] <10>

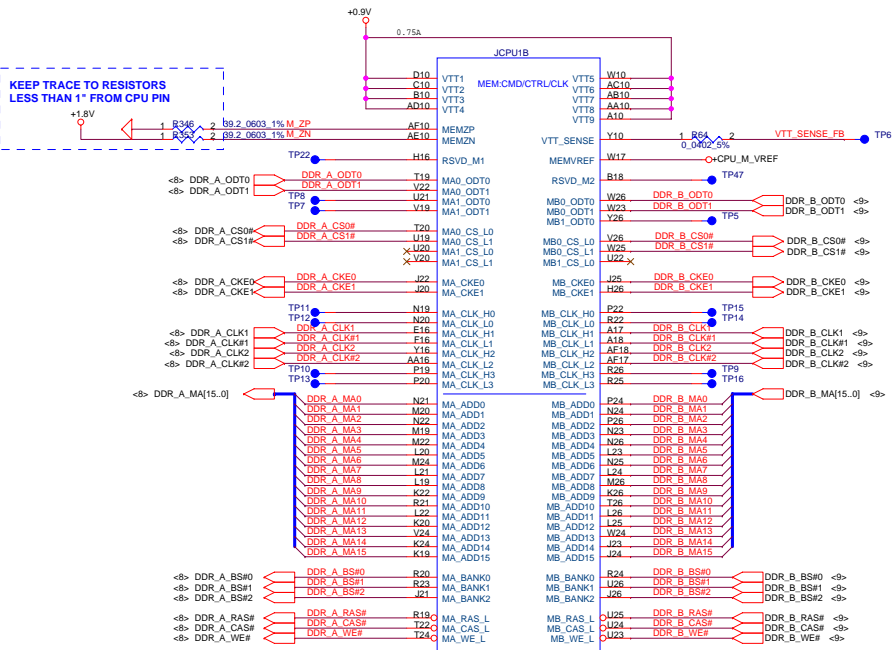


### FAN1 Control and Tachometer

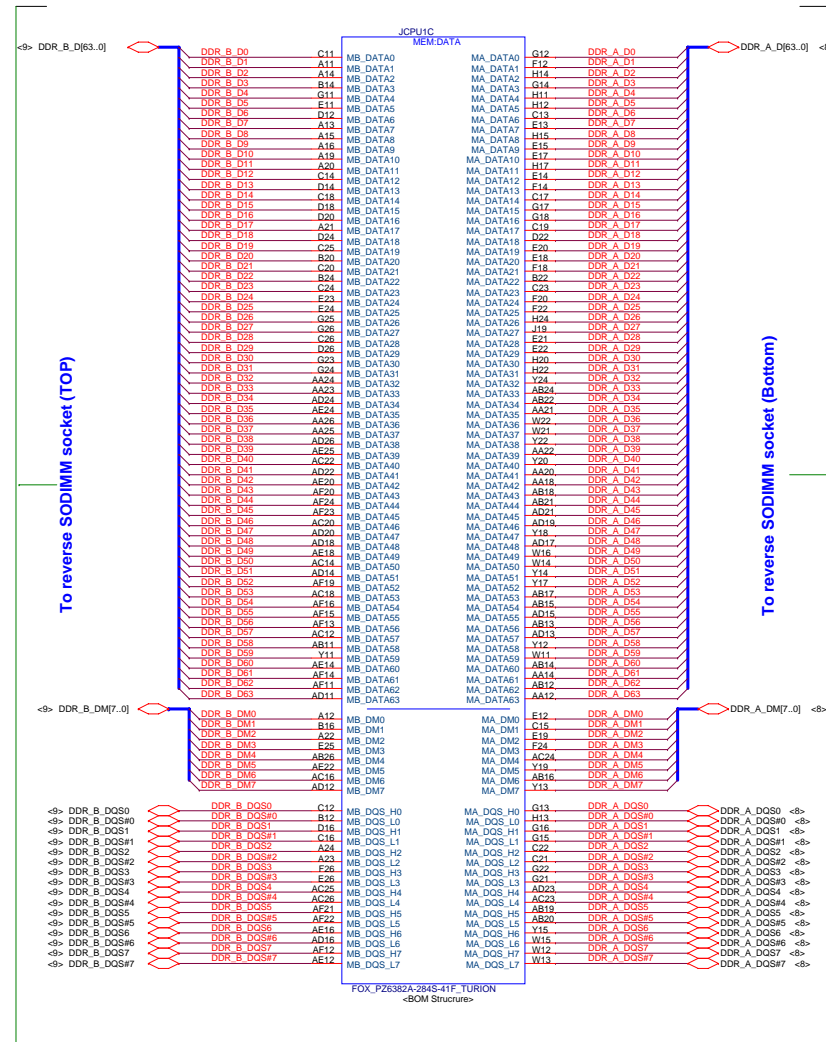


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VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

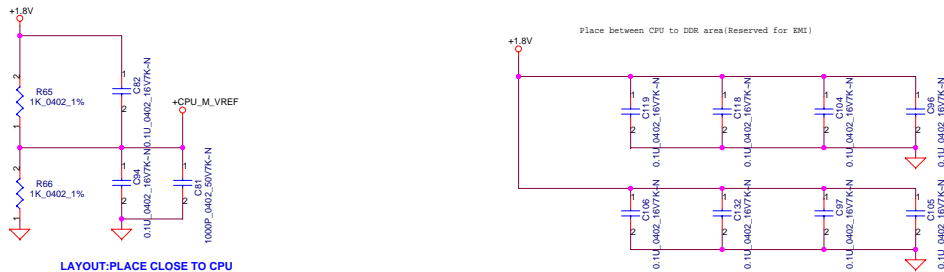


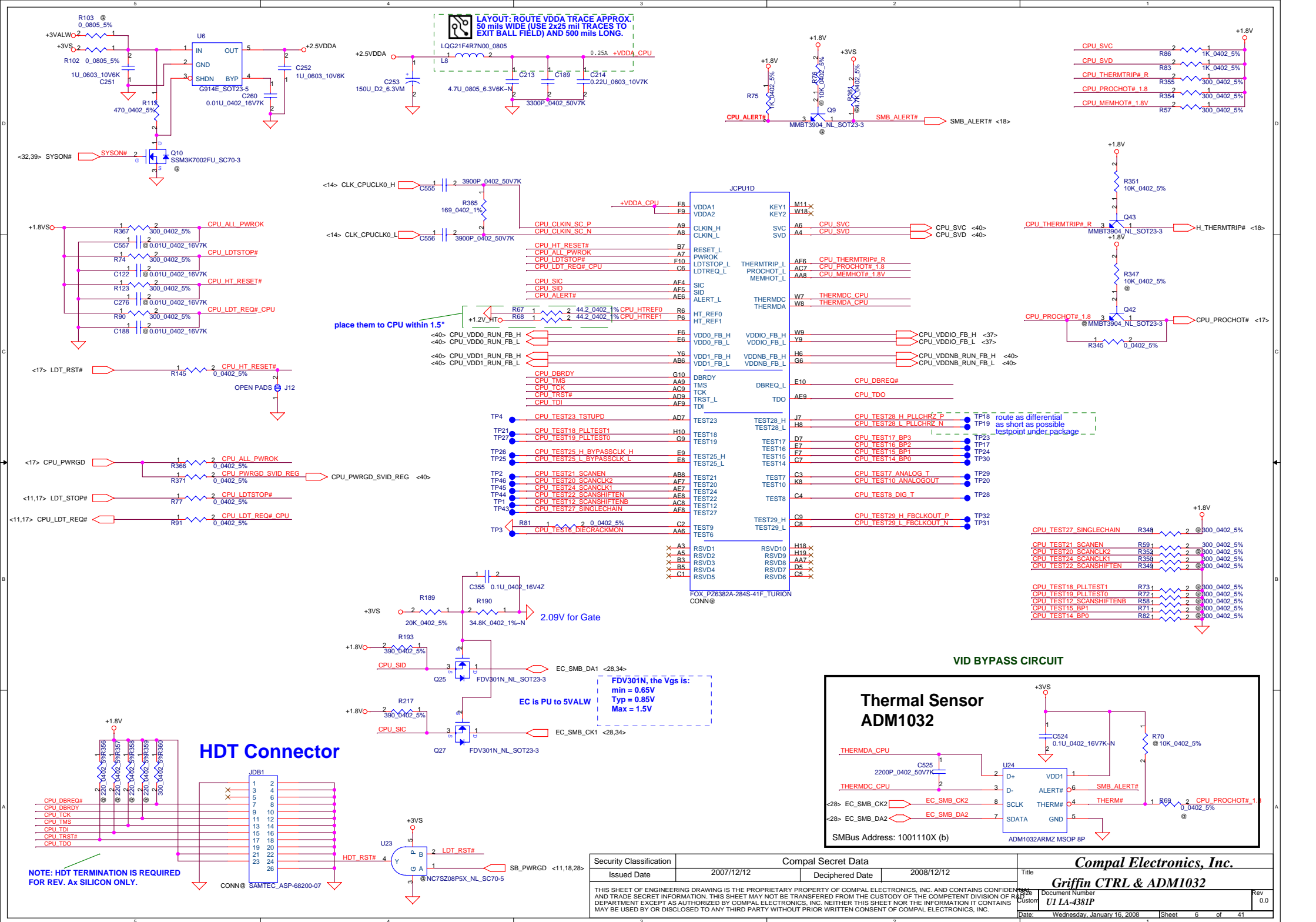
## Processor DDR2 Memory Interface



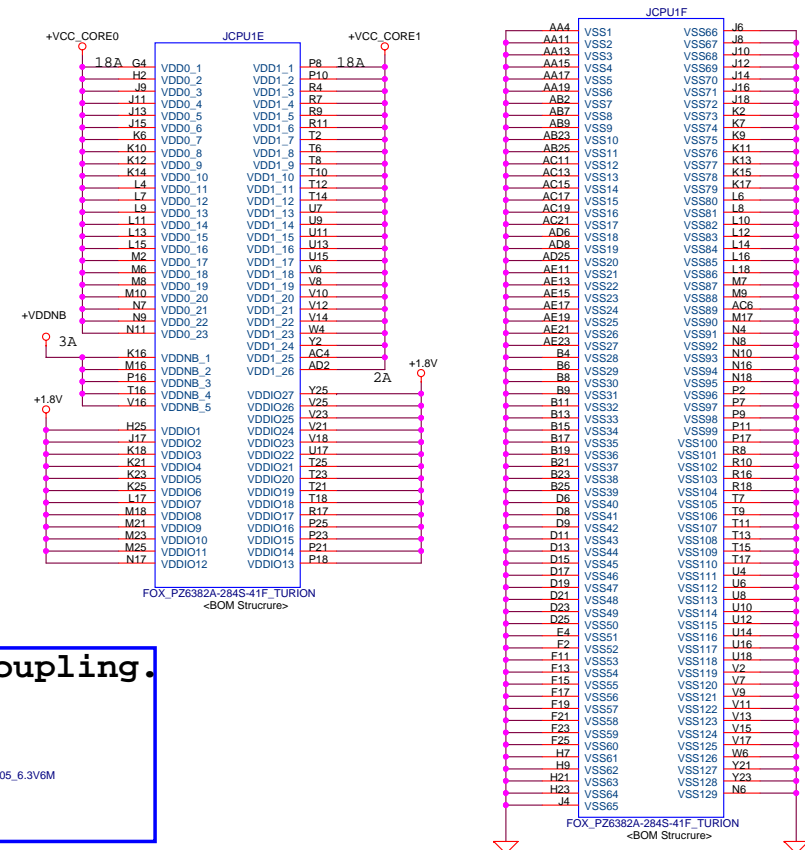
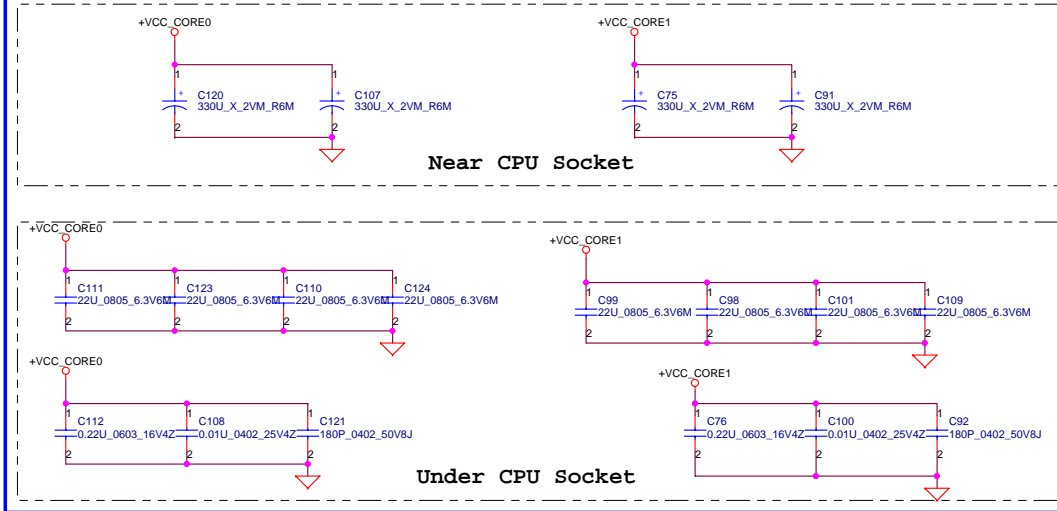
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH

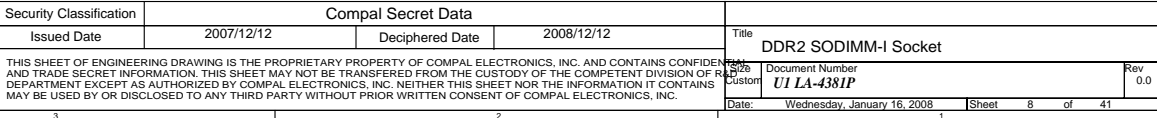
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



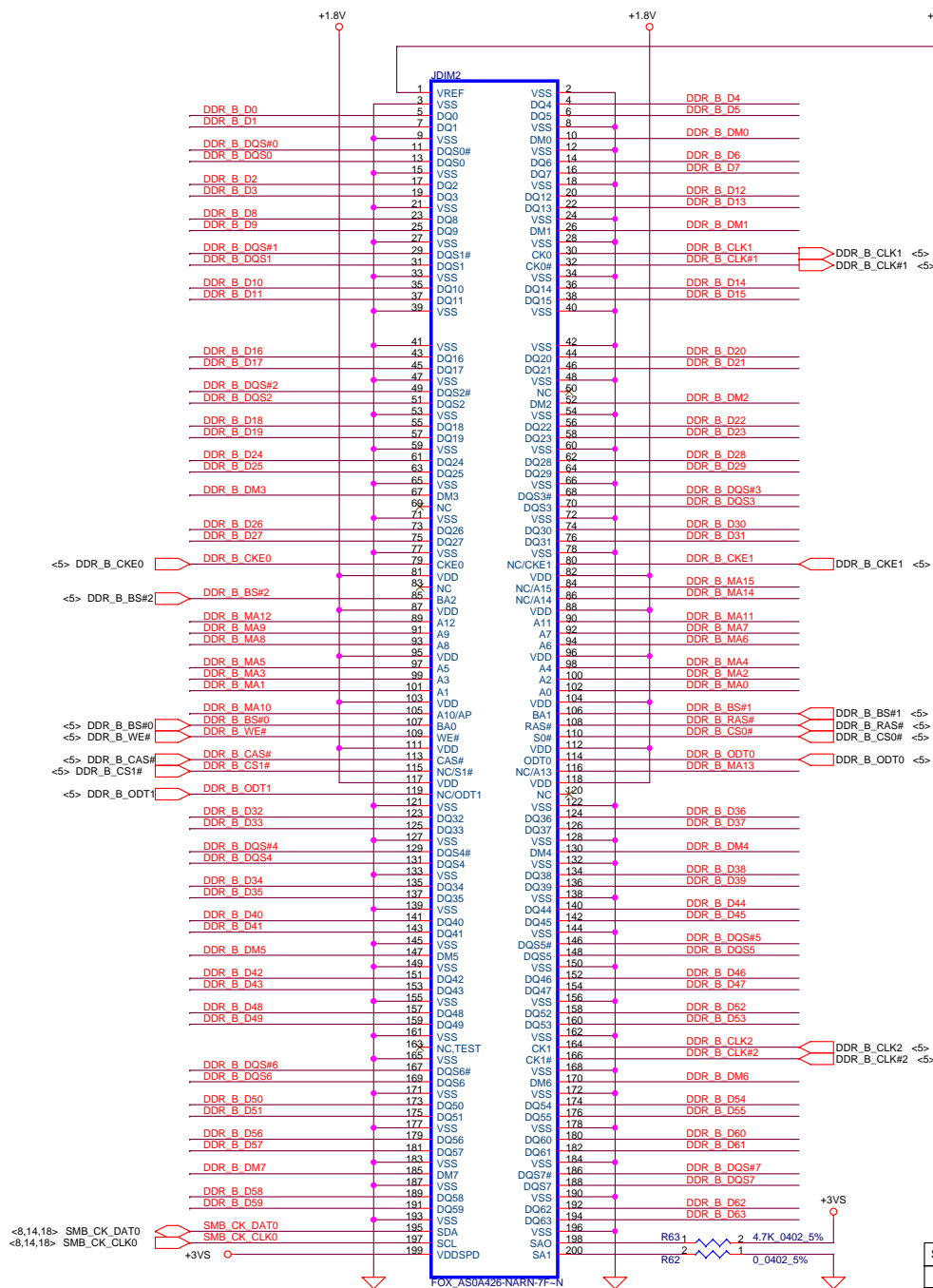


## VDD(+CPU\_CORE) decoupling.

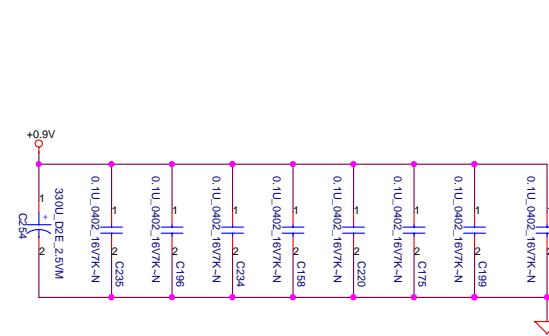
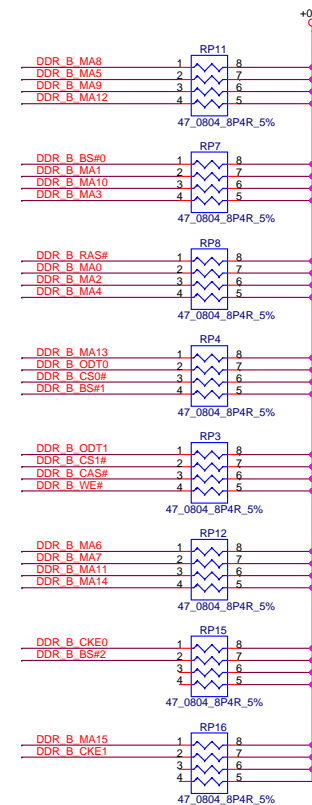




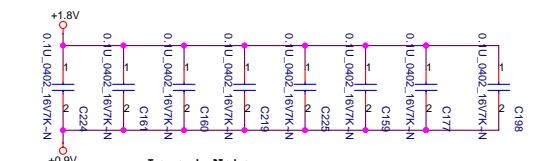




- <5> DDR\_B\_D[0..63]
- <5> DDR\_B\_DM[0..7]
- <5> DDR\_B\_DQS[0..7]
- <5> DDR\_B\_MA[0..15]
- <5> DDR\_B\_DQS# [0..7]

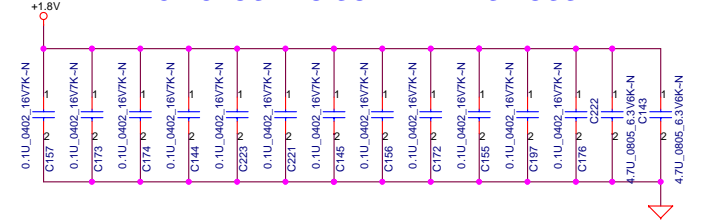


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V

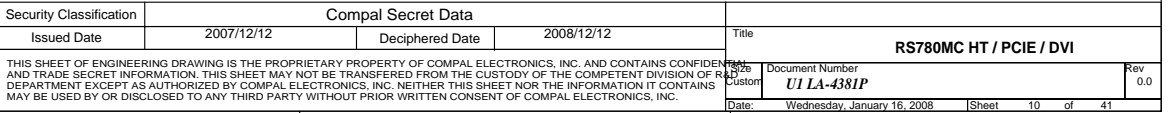


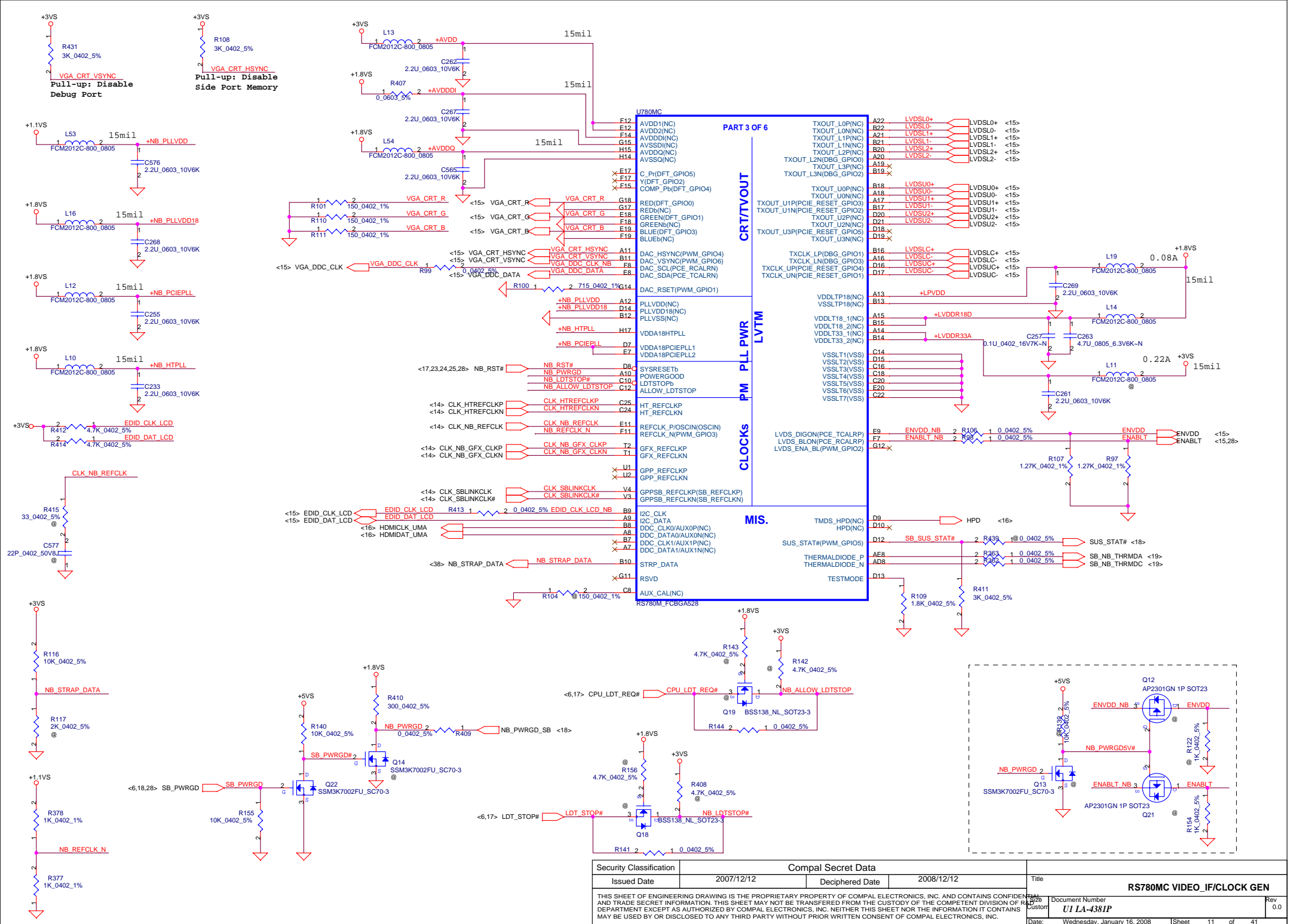
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V

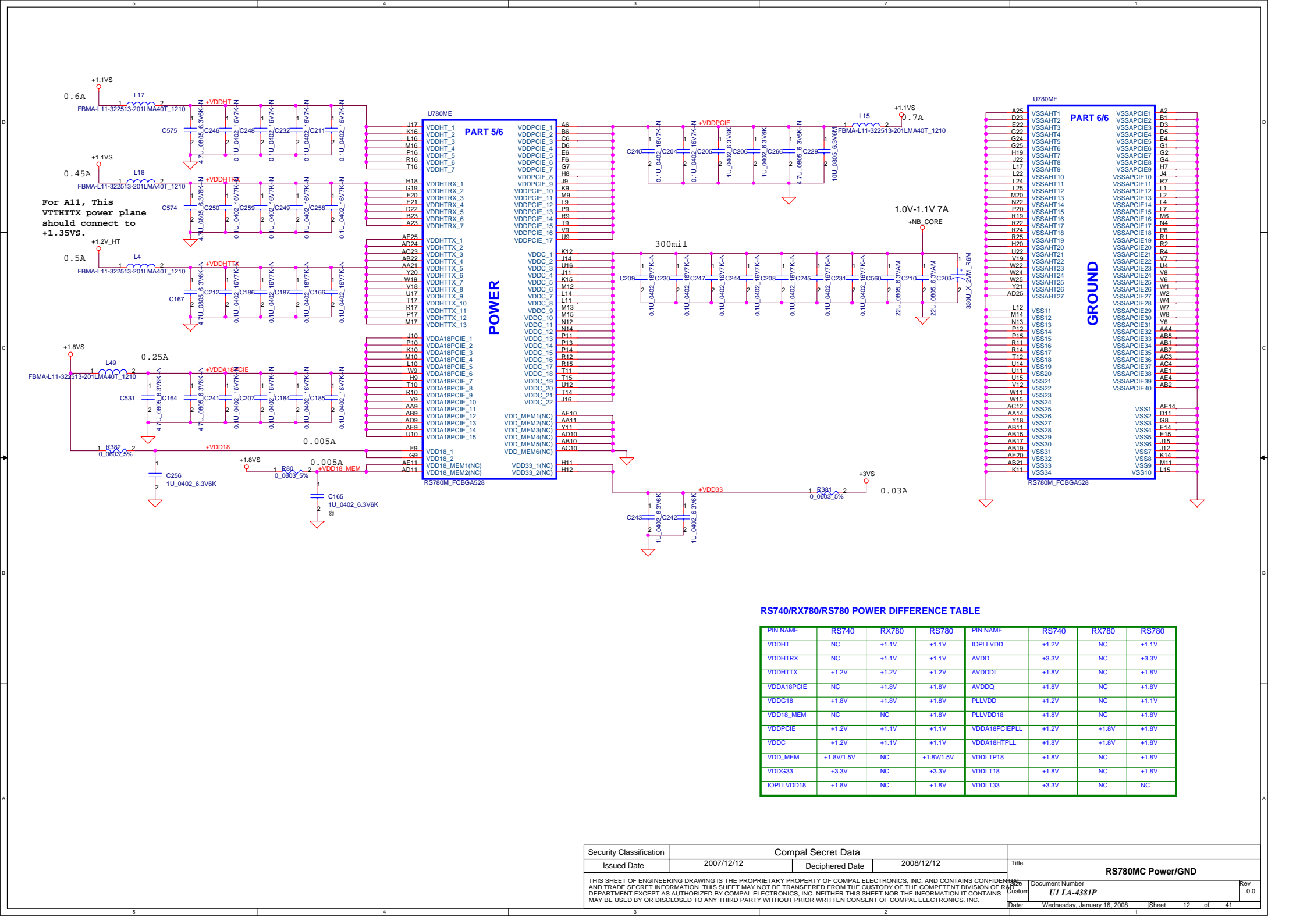
**PLACE CLOSE TO SO-DIMM2 AS POSSIBLE**



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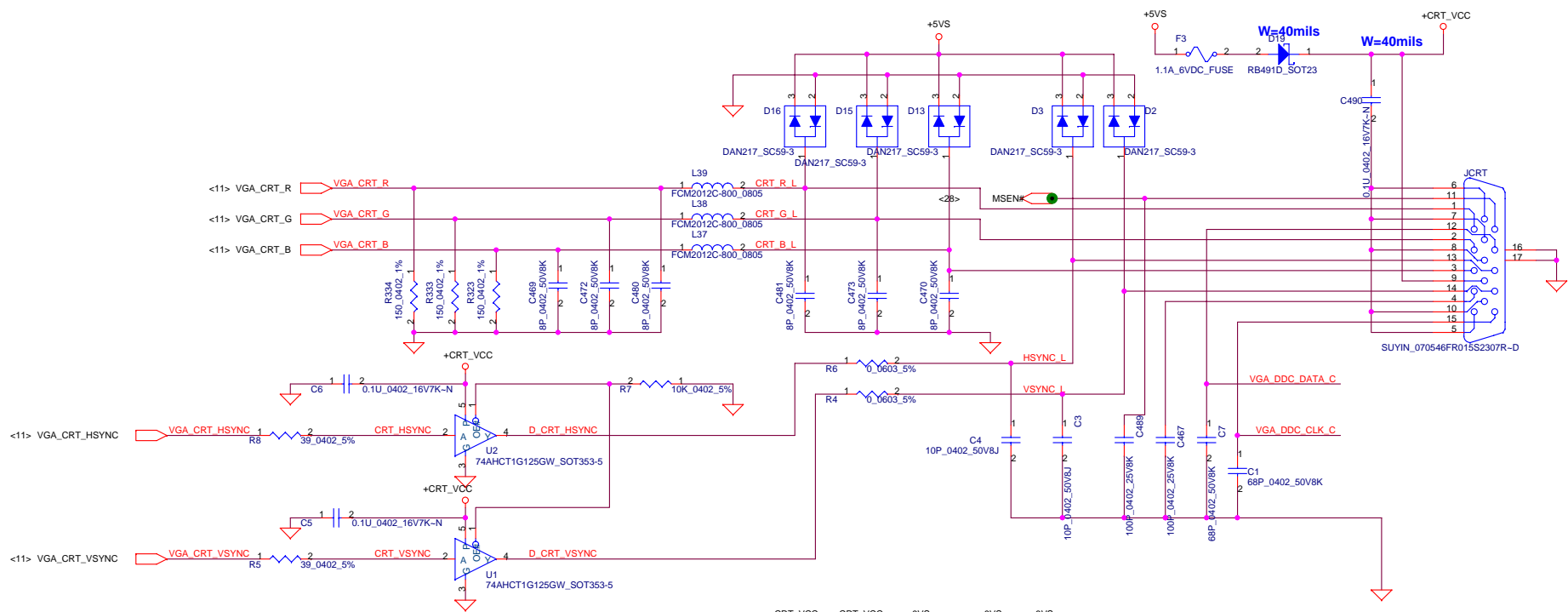




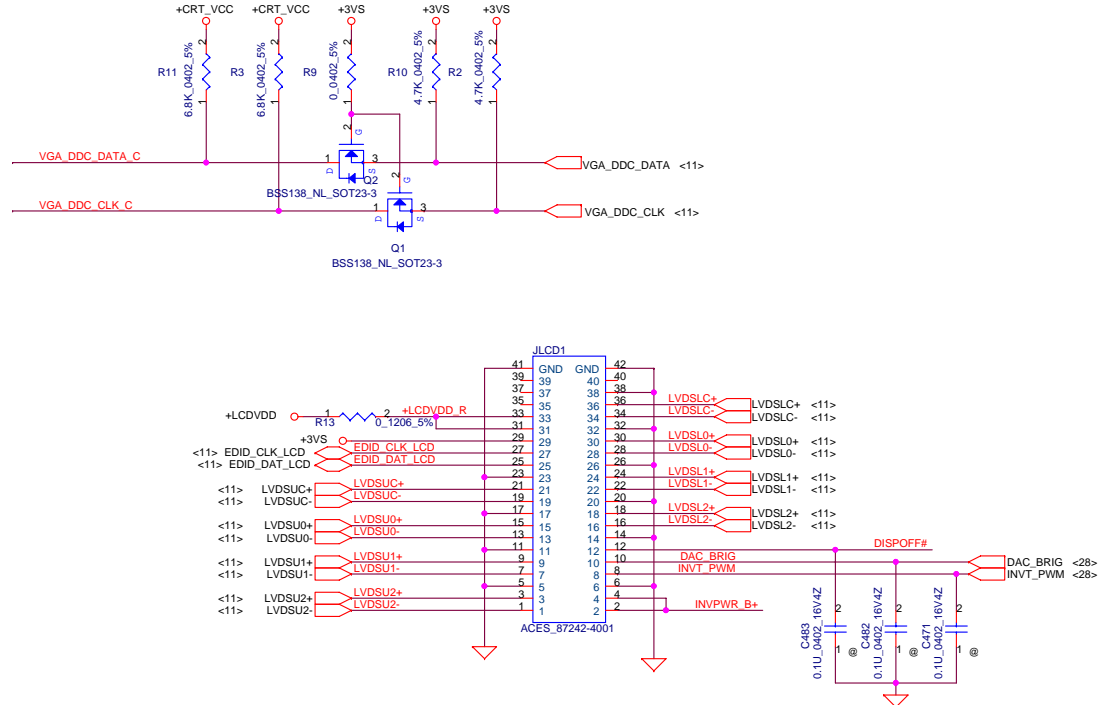
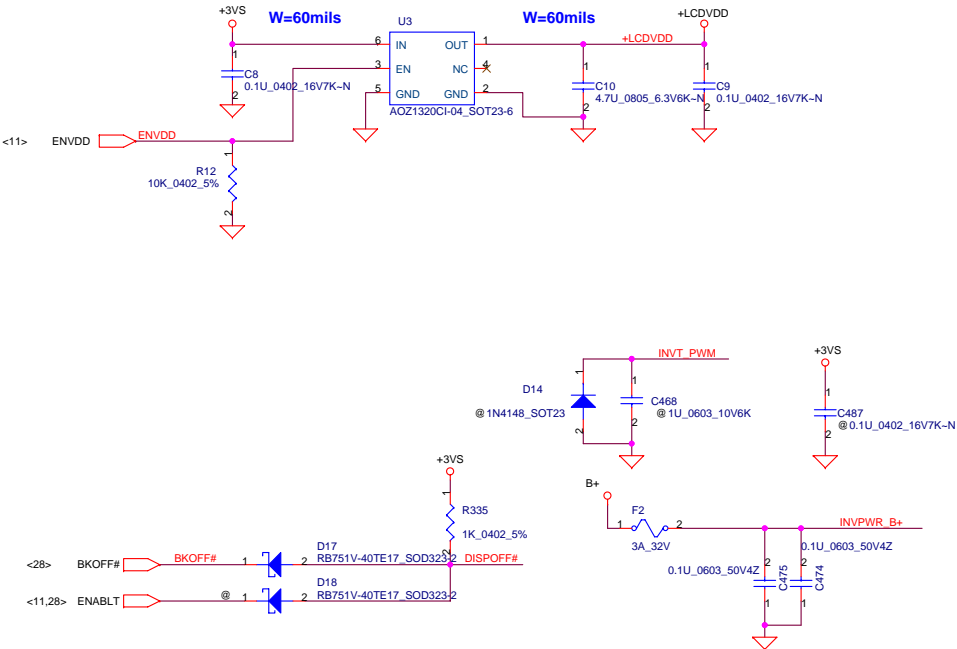








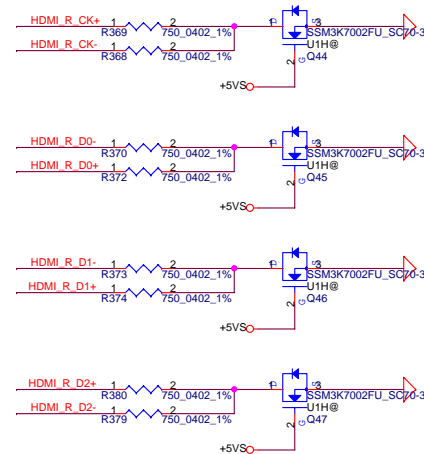
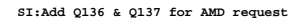
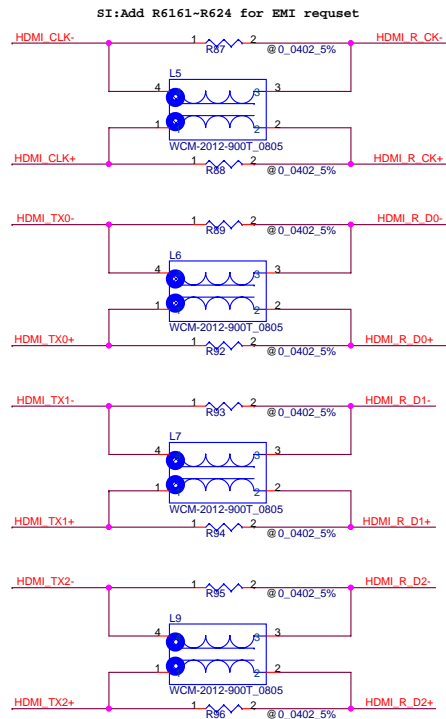
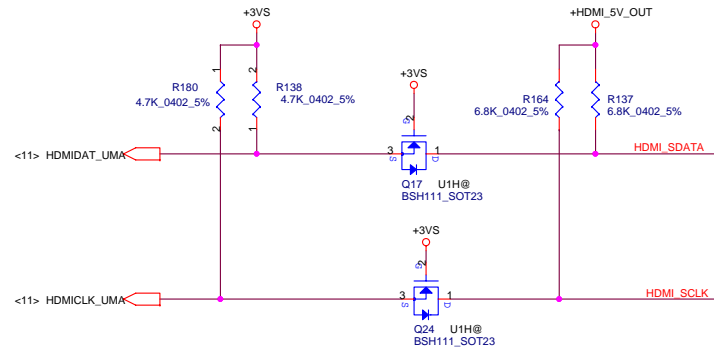
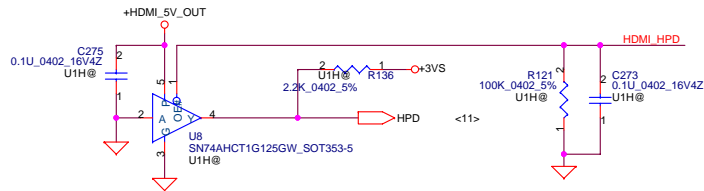
### LCD POWER CIRCUIT



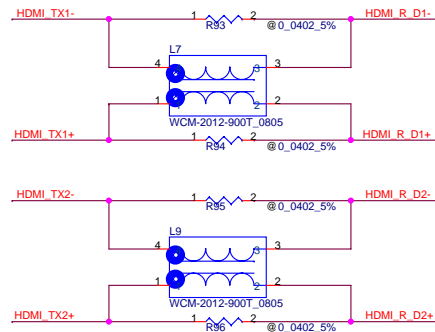
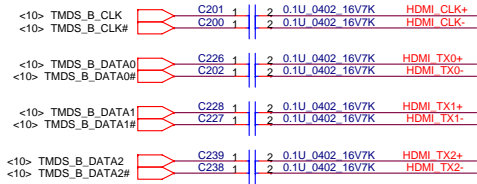
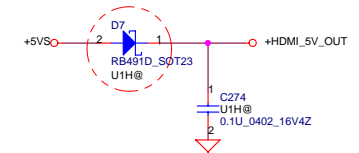
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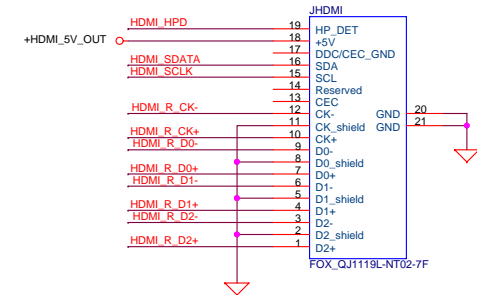
**FOR U1H**



MP:Update D10 to meet HDMI.

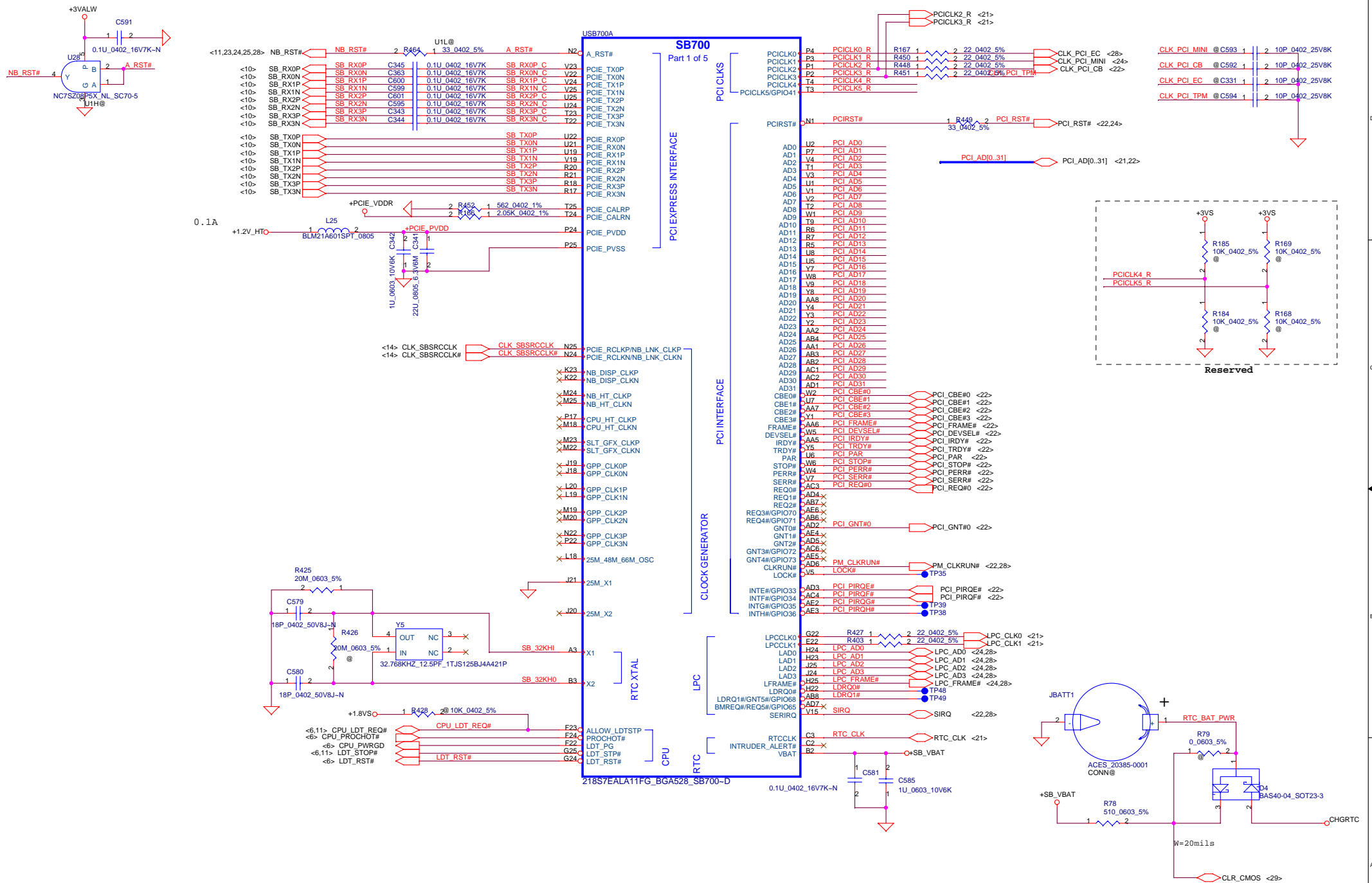


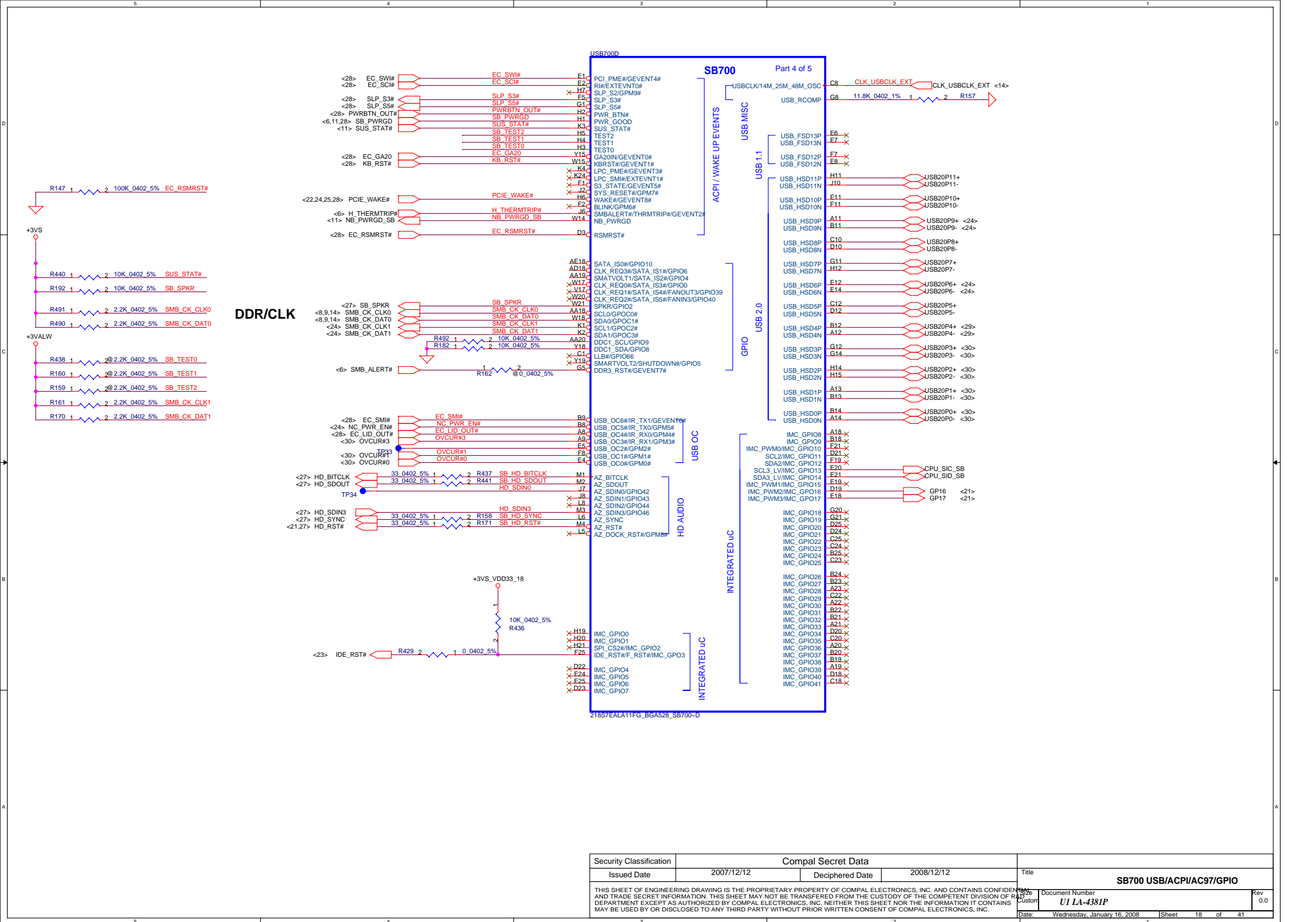
## HDMI Connector



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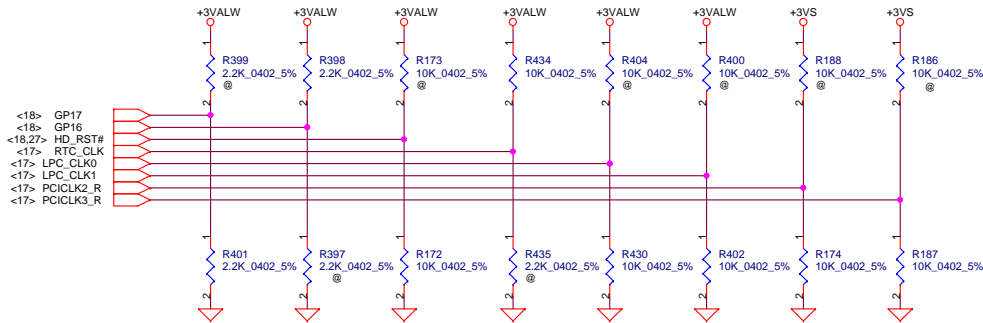


	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT  DEFAULT	CLKGEN DISABLED  DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.  
I.E. LPC\_CLK0 FOR EC ENABLE, AZ\_RST# FOR MEM BOOT ENABLE.



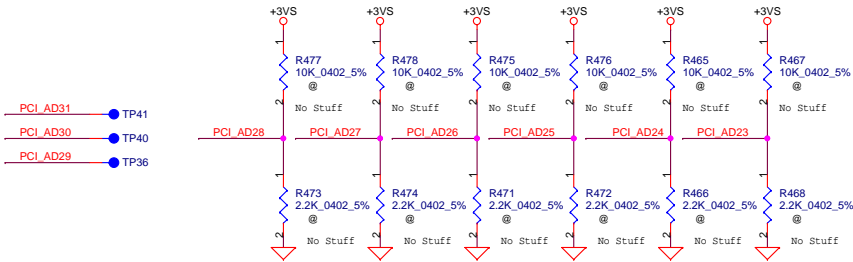
## REQUIRED STRAPS



## DEBUG STRAPS

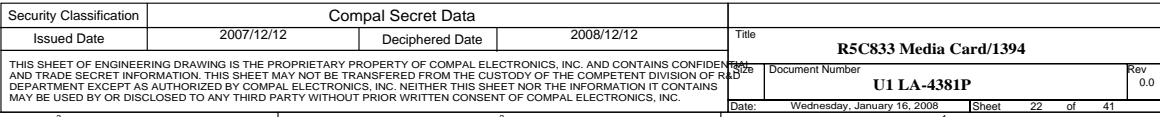
PCI\_AD[0..31] PCI\_AD[0..31] <17,22>

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	RESERVED
PULL LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

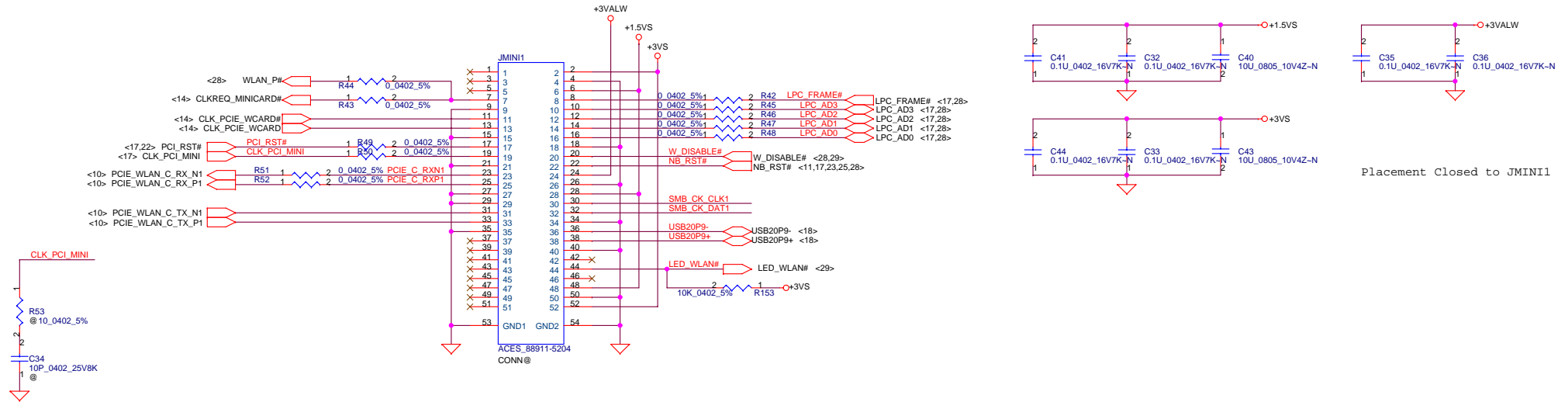
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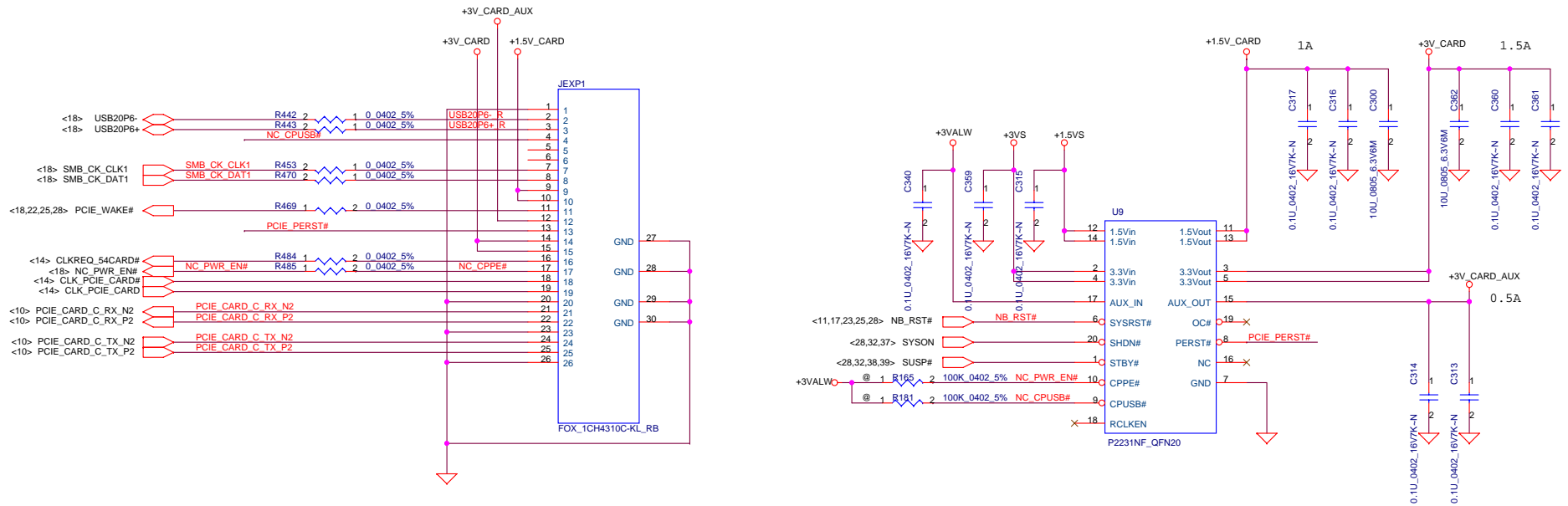
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## Mini-Express Card

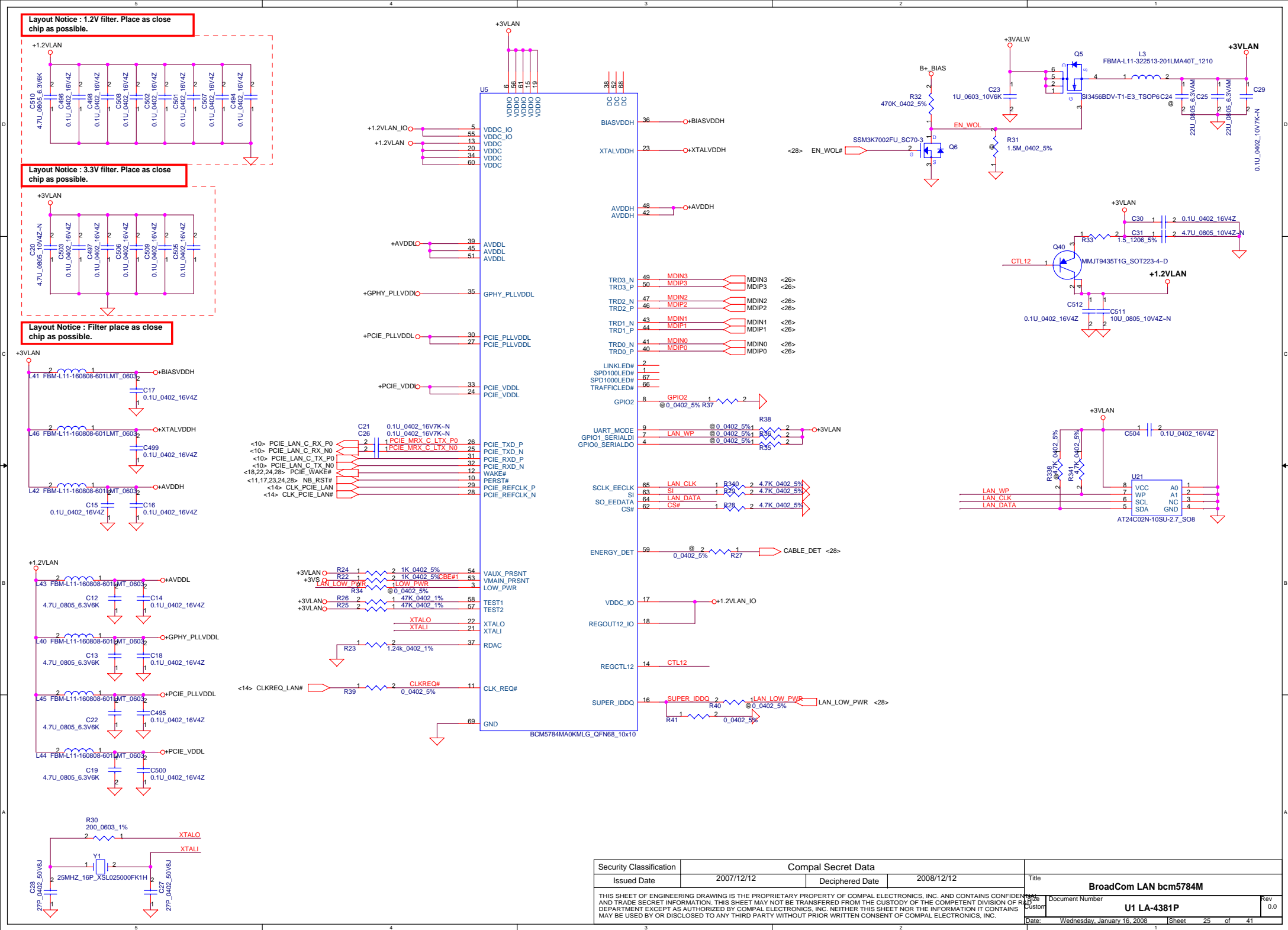


## New Card

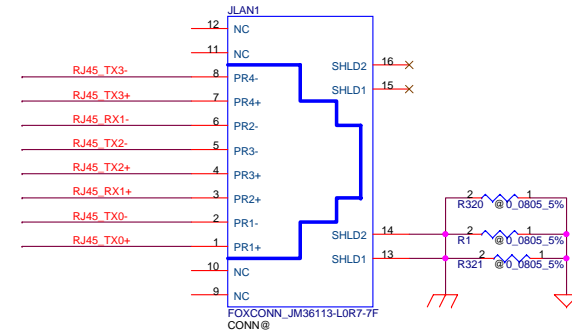
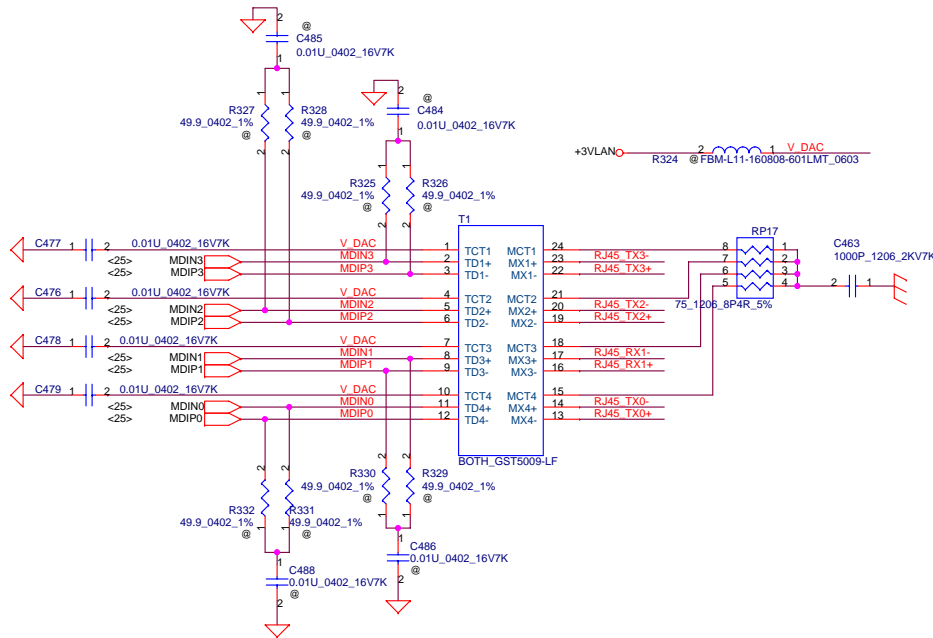


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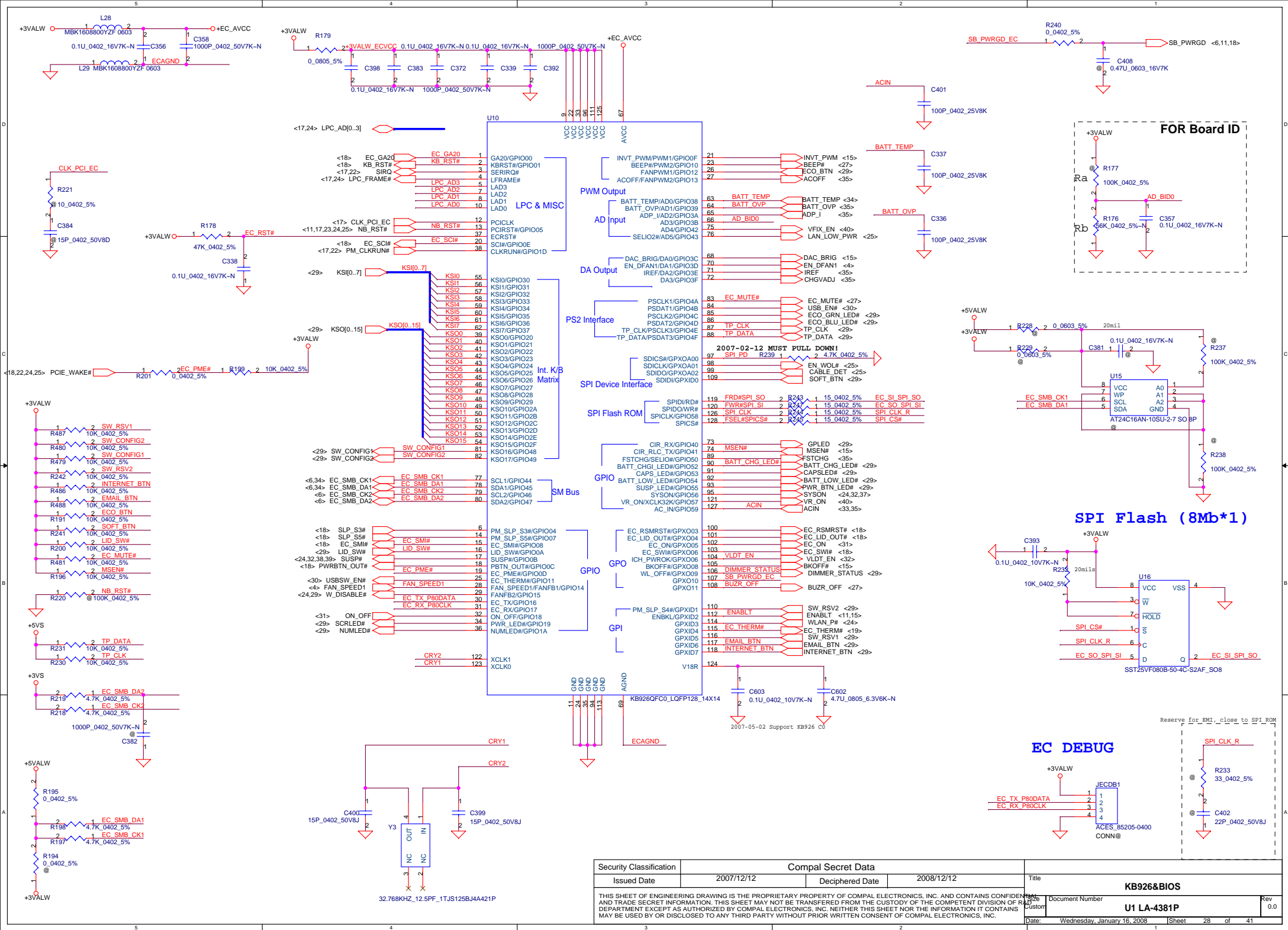


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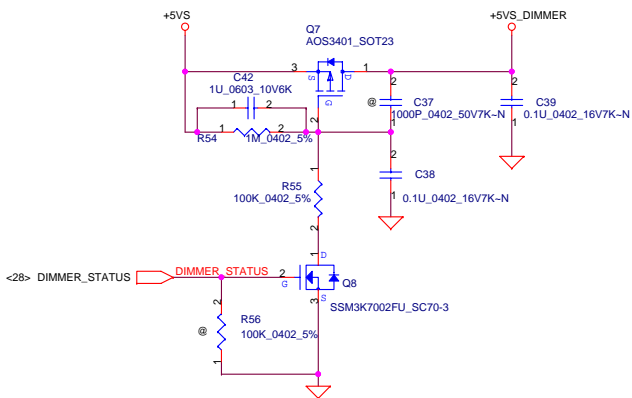
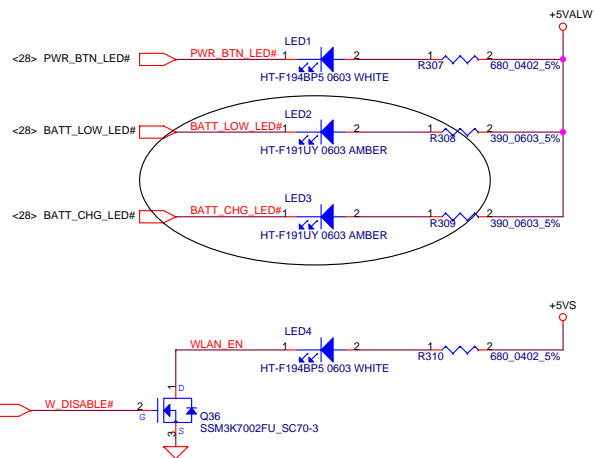
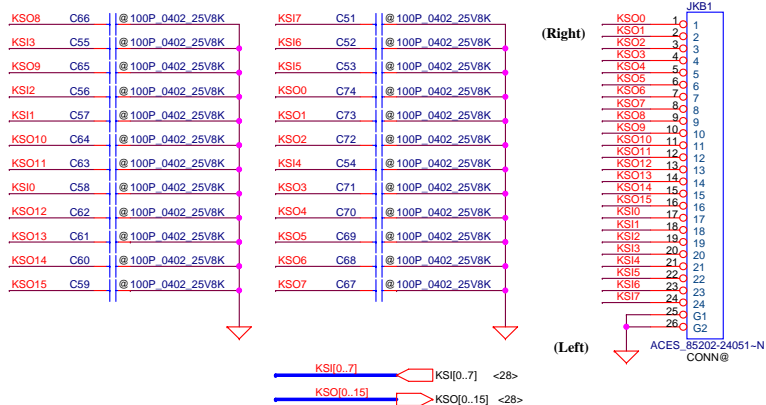
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								Custor		U1 LA-4381P		0.0	
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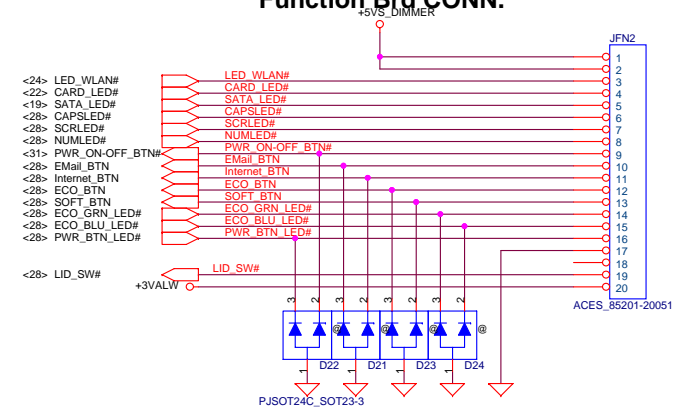


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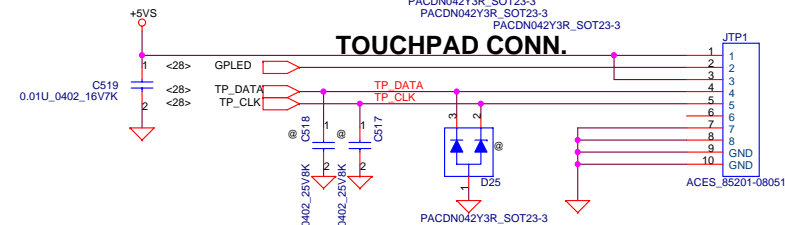
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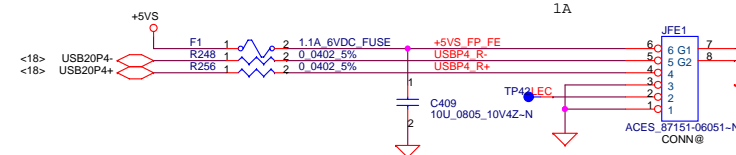
## Function Brd CONN.



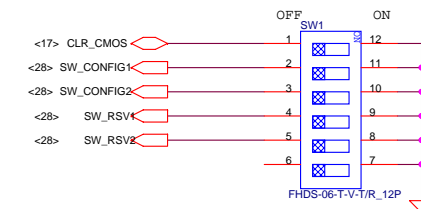
## TOUCHPAD CONN.



## Felica CONN.

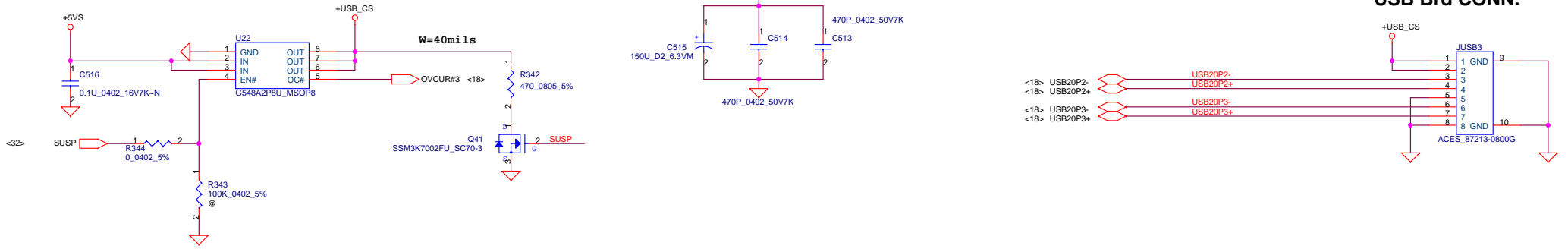
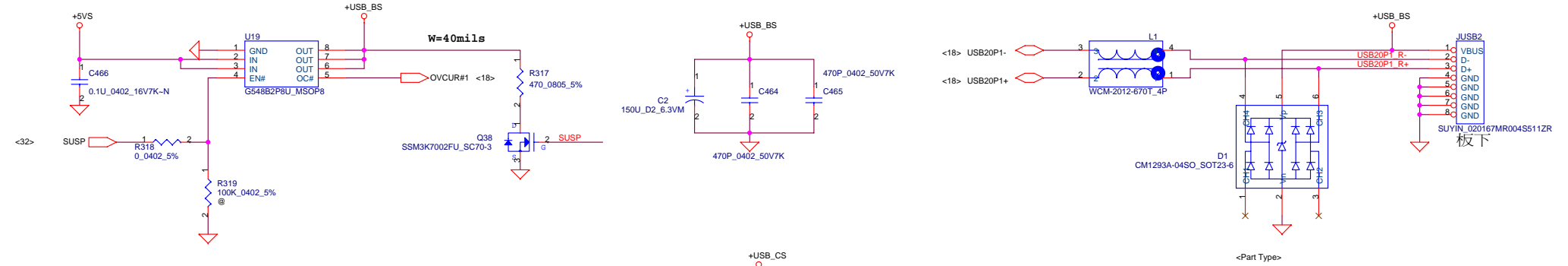
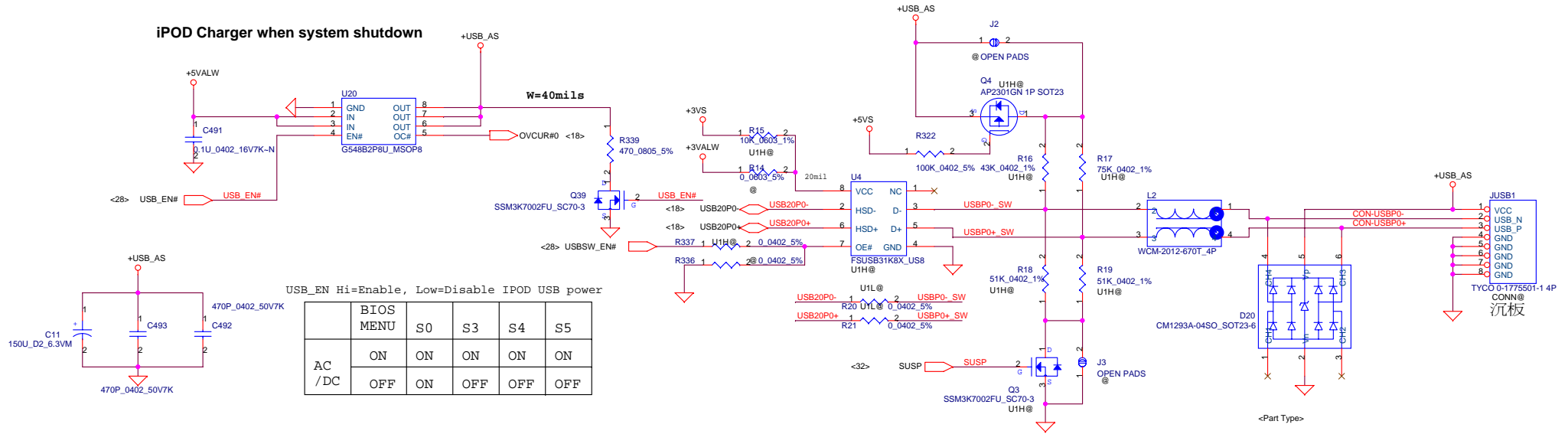


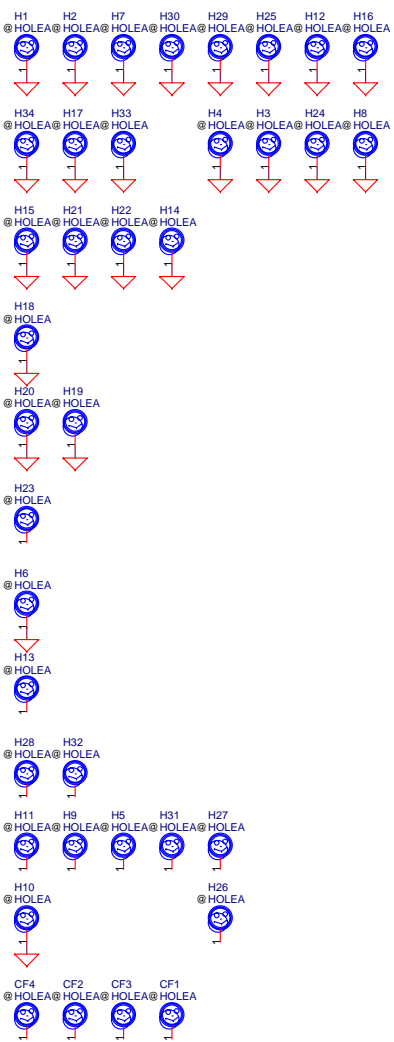
## Dip Switch CONN.



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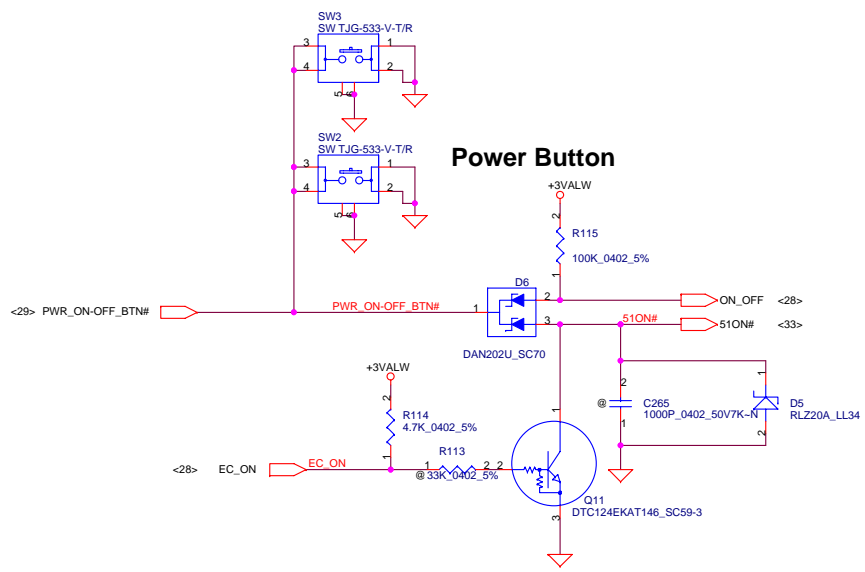
# iPOD Charger when system shutdown





H\_3P0

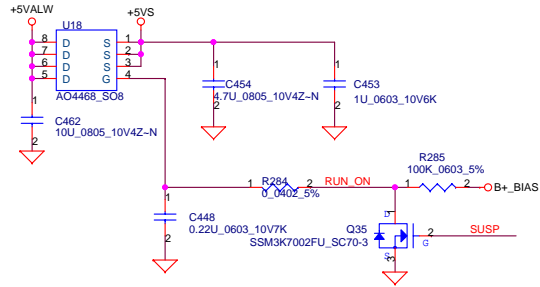
H\_4P2



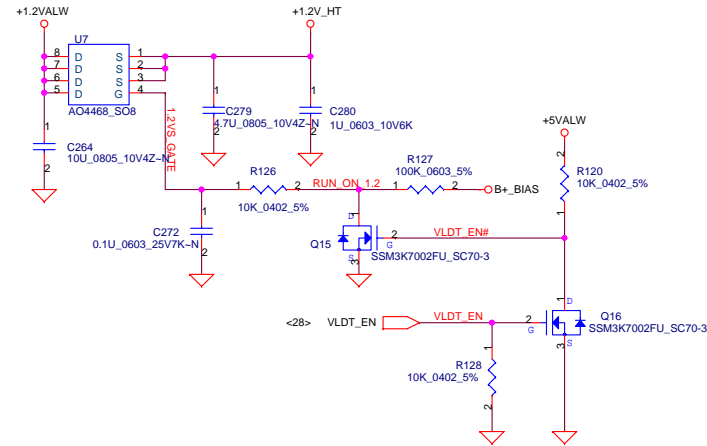
### Power Button

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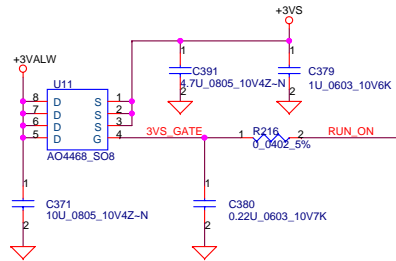
**+5VALW TO +5VS**



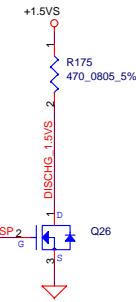
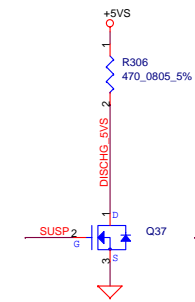
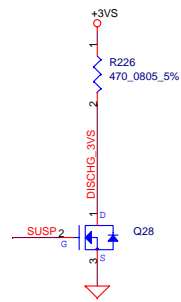
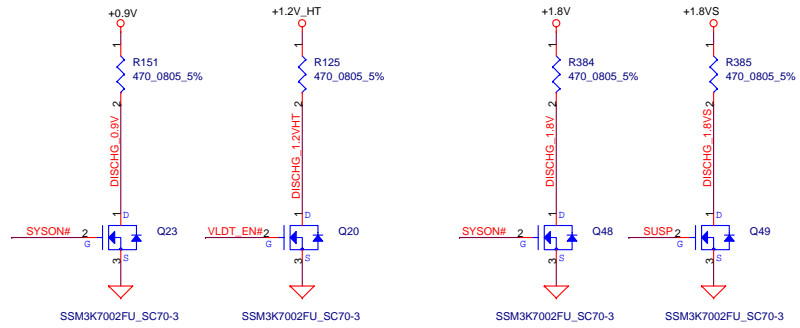
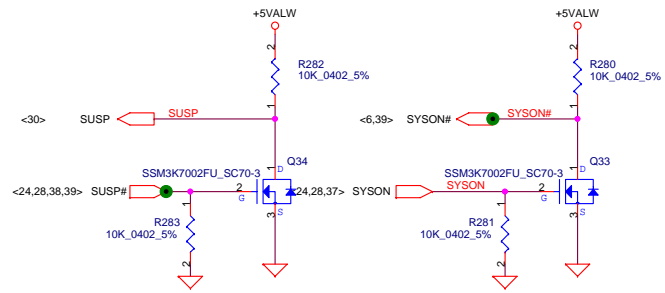
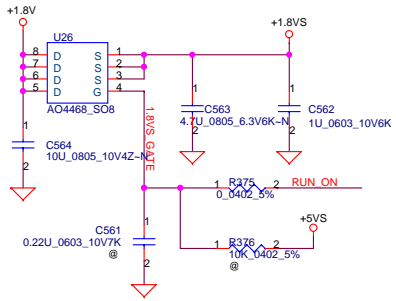
**+1.2VALW TO +1.2V\_HT**



**+3VALW TO +3VS**



**+1.8V TO +1.8VS**



SSM3K7002FU SC70-3		SSM3K7002FU SC70-3		SSM3K7002FU SC70-3					
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						Title			
						DC Interface			
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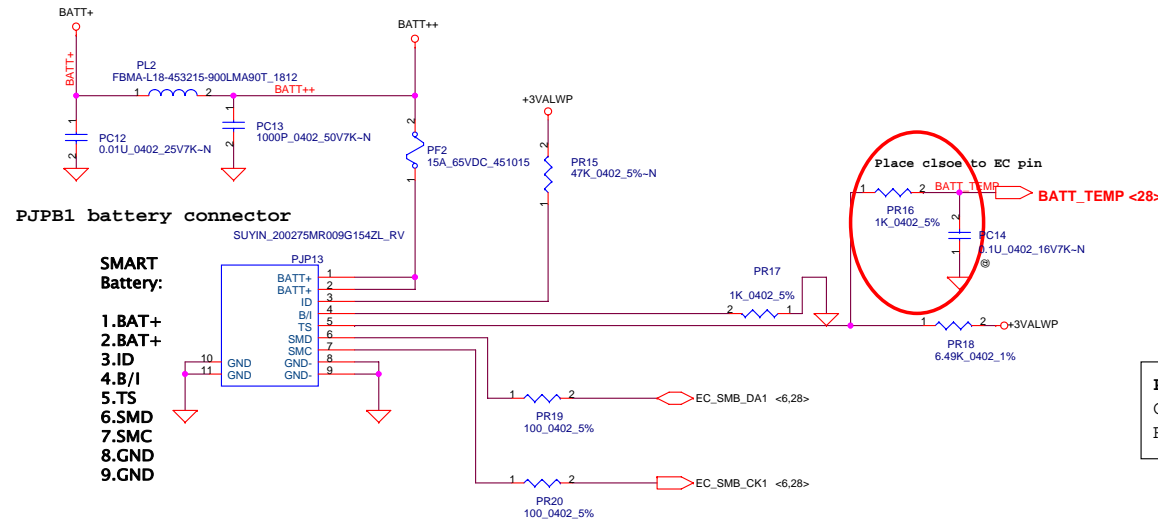


Vin Detector			
High	14.57	14.01	13.46
Low	14.06	13.51	12.98

High	14.57	14.01	13.46
Low	14.06	13.51	12.98

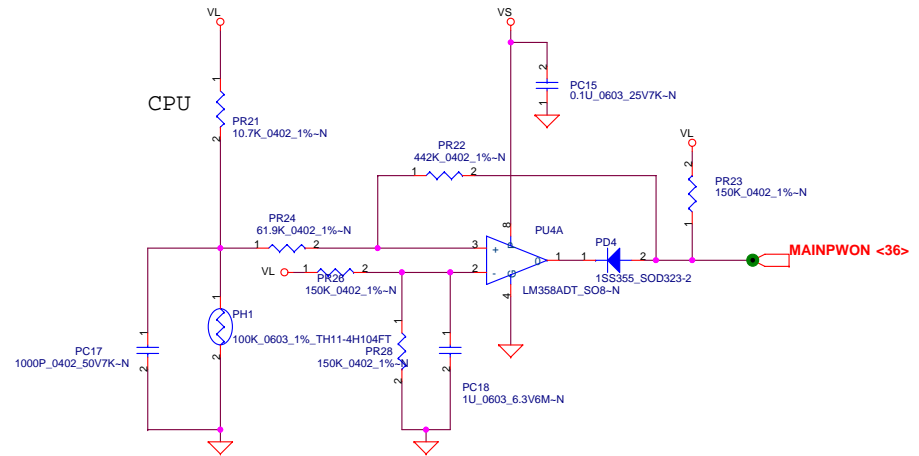
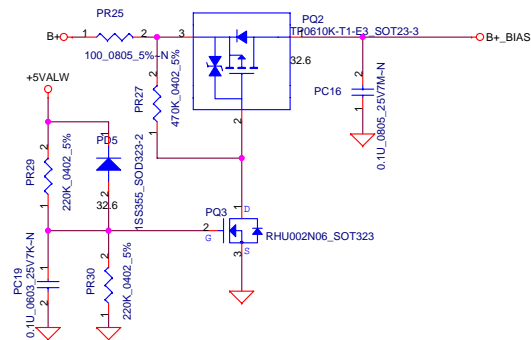
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## Battery Connect/OTP

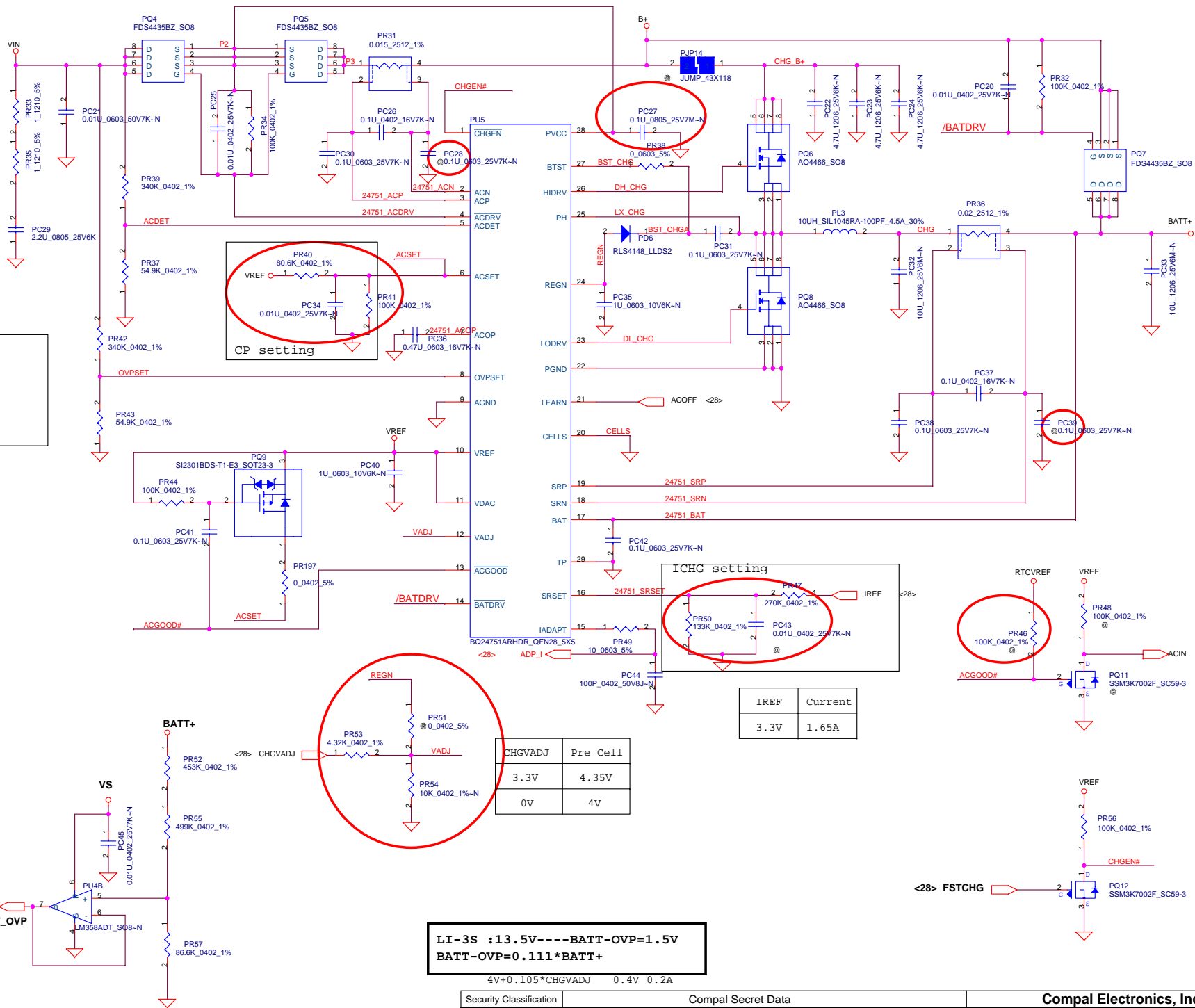


### CPU

**PH1 under CPU bottom side :**  
CPU thermal protection at 90  $\pm$  3 degree C  
Recovery at 50  $\pm$  3 degree C



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CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

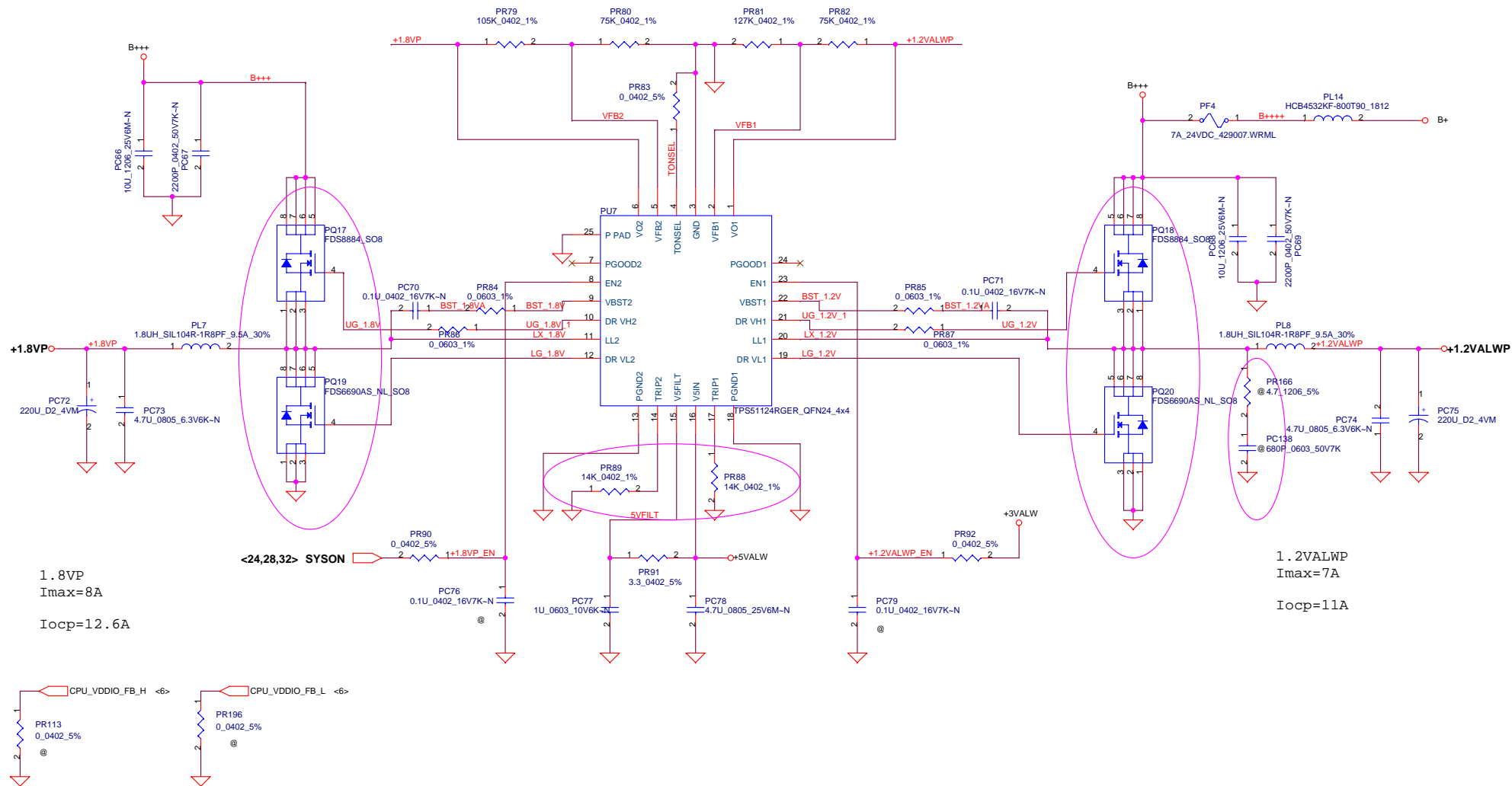
IREF	Current
3.3V	1.65A

---

4V+0.105\*CHGVADJ      0.4V 0.2A

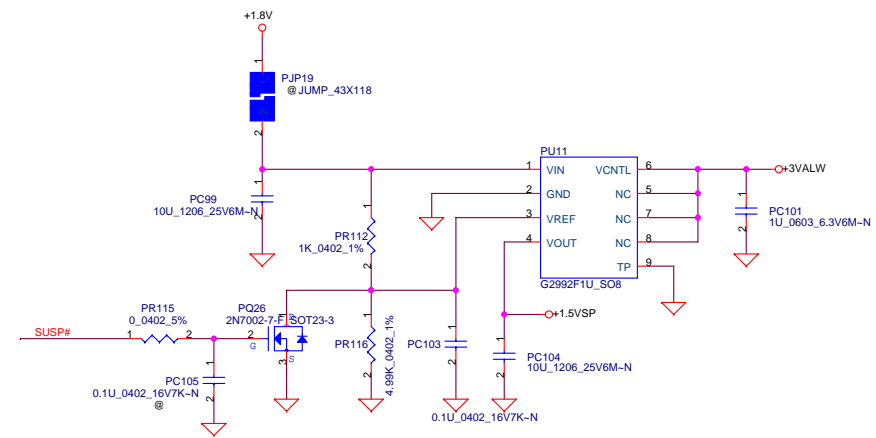
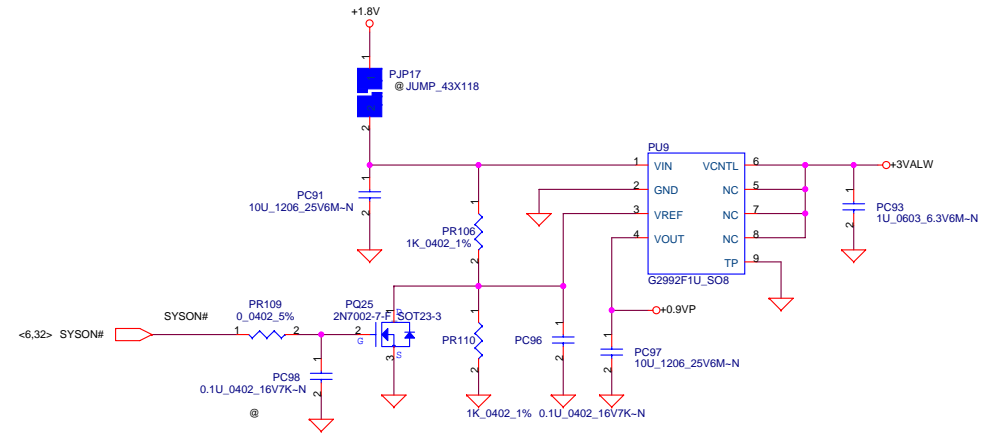
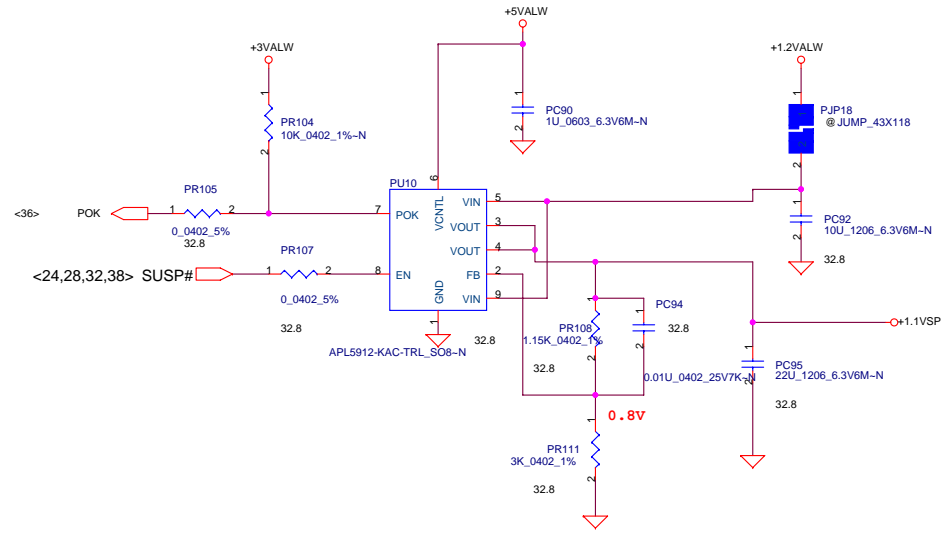
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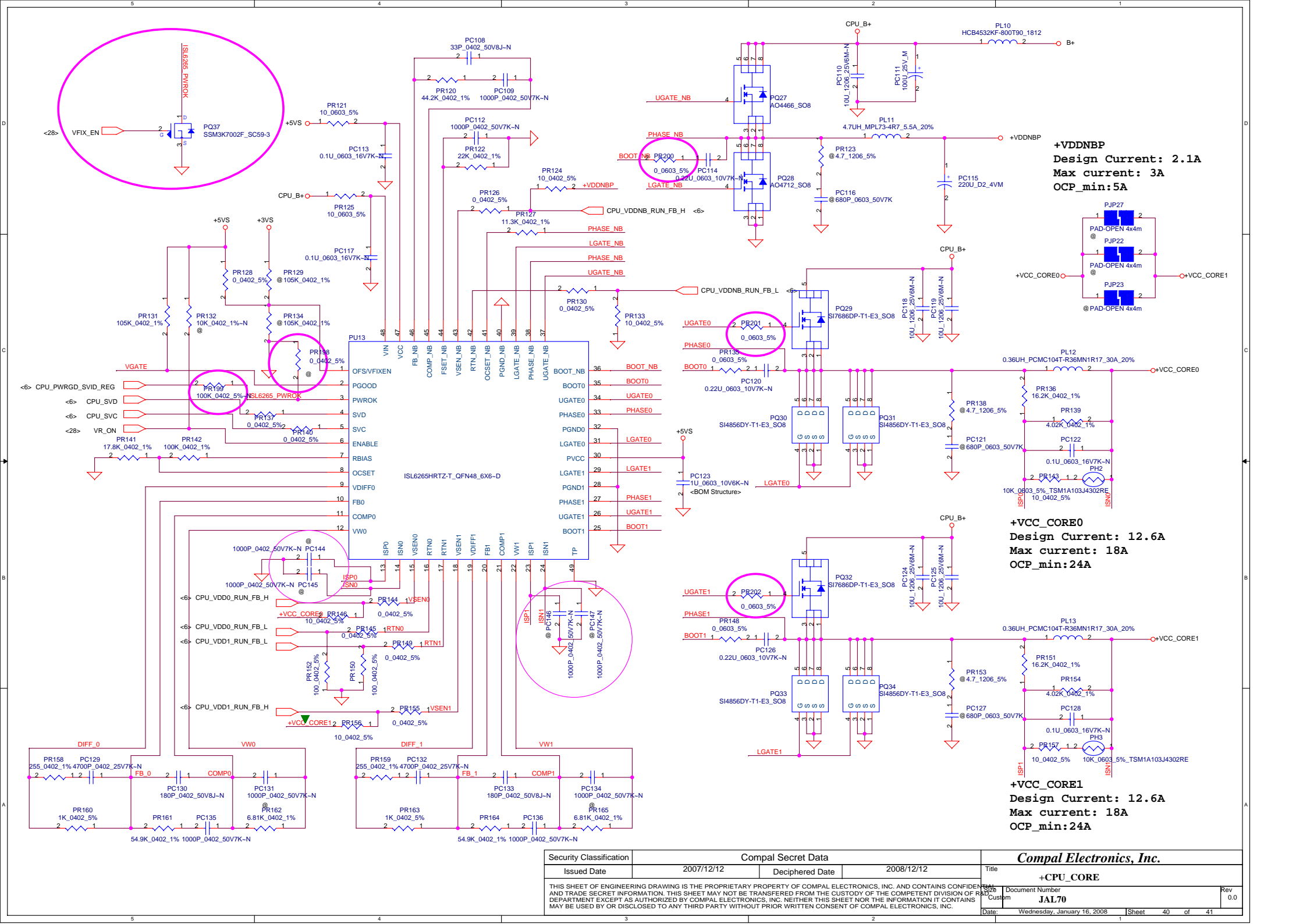


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				Document Number			
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Title			
<h2 style="text-align: center;">EE-PIR</h2>			
Drawing Number			Rev
<h1 style="text-align: center;">UT LA-4381P</h1>			0.0
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